Errata (updated June 25, 2011)

p. 278, Equations (7.16a), (7.16b). No negative sign to the right of the equal sign.

p. 308, Equation (7.114a). Should read:

$$\texttt{be\_y(j) = exp(-(}\sigma_y^e\texttt{(j)/}\kappa_y^e\texttt{(j) +}\, a_y^e\texttt{(j)) * }\,\Delta t/\varepsilon_0) \qquad (7.114a)$$

p. 309, Equation (7.118a). Should read:

$$\texttt{bh\_y(j) = exp(-(}\sigma_y^h\texttt{(j)/}\kappa_y^h\texttt{(j) +}\, a_y^h\texttt{(j)) * }\,\Delta t/\varepsilon_0) \qquad (7.118a)$$

p. 337, second line from the bottom. Should read: Chapter 15, Section 15.8

p. 369, 3rd paragraph. Should read: Polder tensor

p. 465, Equation (11.8). The superscript of M_z should be n, not n+1/2.

p. 465, Equation (11.9). The denominator of the σ-related term should be 2, not 2Δt.

p. 467, Equation (11.10). The superscript of M_z should be n, not n+1/2.

pp. 526, 527: In Equations (12.24) and (12.30), r_1 in the numerator of the second term of the right-hand side should be r_2.

p. 527: The + sign in front of the last term on the right-hand sides of Equations (12.27) and (12.30) should be a – sign.

p. 900, Equations (18A.1) and (18A.2). Should read:

$$\int_0^\tau e^{u[L]}\{S(t+\tau-u)\}du = \tau\sum_{i=1}^{n} w_i e^{(1+x_i)\tau[L]/2}\{S(t+(1-x_i)\tau/2)\} + O(\tau^{2n+1}) \qquad (18A.1)$$

$$\int_0^{\tau} e^{u[L]}\{S(t+\tau-u)\}du = \tau\sum_{i=1}^{n} f[t+(1-x_i)\tau/2]w_i e^{(1+x_i)\tau[L]/2}\{S_0\} \qquad (18A.2)$$

p. 957, Point 5. Should read:

5. References [13–15] reported what appear to be the first successful three-dimensional FDTD accelerators to be implemented in physical hardware. Here, as stated in [14], "the front-end software sends the appropriate data, such as the mesh size and the number of time-steps to execute, to the hardware via the PCI bus. The FDTD accelerator proceeds to update the fields, periodically sending the results back to the host computer for postprocessing and visualization." In the most recent work of this group, updating throughputs as high as 30 million three-dimensional cells per second were achieved using a custom circuit board and FPGA implementation.